Design and Implementation of novel XOR gate, Adder and Subtractor circuit using Quantum dot Cellular Automata Technology

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Abstract*— The QCA operation at frequencies in the THz range and device incorporation densities roughly 900 times higher is making over as well as improving the limitations of current CMOS technology. The QCA layout takes advantage of emerging technologies like mobile ram and processor via wires. The CAD tool, i.e. QCADesigner is used for design and simulation. Cells have a dimension of 18 nm in height and 18 nm in breadth and there is a distance of 2 nm between these cells. Bi-stable and coherence vector simulation engines are used in the tool for simulation. In this paper, we will successfully design, implement and simulate a new 2-input XOR gate (exclusive OR gate) based on QCA with the minimum delay, area and complexities. Then, we will use XOR gates presented in this paper, in an adder and subtractor circuit. This circuit is more efficient in terms of cell count energy dissipation, and area occupied by the logical circuit.

***Index Terms*—Basic QCA, Coherence Vector Simulation Engine (CVSE), Majority Voter (MV), Nand-Nor-Inverter (NNI).**

I. INTRODUCTION

The International Technological Roadmap for Semiconductors (ITRS) announced portable death of Moore's law in last decade in 2015. The primary tendency towards achieving fast-speed, high-density, low-power-dissipating circuit is to reduce the number of transistors used in circuit. On the other hand, several issues arise when scaling reaches the submicron range. Researchers have proposed a new computer paradigm using quantum dots i.e. Quantum dot Cellular Automata as an alternative to CMOS -VLSI. The quantum-dot cellular automata (QCA) introduced by Lent et al. (1993) [1] is a nanostructure paradigm that uses arrays of connected quantum dots to accomplish Boolean logic functions. QCA is based upon the encoding of binary information in the charge configuration within quantum dot cells. Computational power is provided by the Columbic interaction between QCA cells. The interconnections between cells are provided by the physics of cell-to-cell interaction due to the rearrangement of electron positions.

This paper designs, implements and analyzes a basic device in QCA and use it in one of the most fundamental circuits in QCA. As quantum cells are used in QCA that's why designing method in QCA is very much different from the CMOS. In this paper, 2-input XOR gate with Nand-Nor-Inverter (NNI) have been proposed for implementation in QCA. This 2-input XOR gate is used in designing an adder and subtractor circuit.

II. QCA BASIC

In the Low Power design era Quantum dot cellular automata (QCA) is a leading technology in place of CMOS VLSI design. The QCA technology is based on QCA logic devices: the majority voter (MV), the inverter (INV), binary wire and the inverter chain. Fig. 1 shows the basic QCA cell and logic devices.

The voltage level in CMOS technology is replaced by the polarization of electrons to determine QCA logic state. The two stable polarization of electrons P=+1.00 and P= -1.00 of a QCA cell represents logic '1' and logic '0' respectively.

QCA wires can be either made up of 90^0 cells or 45^0 cells. 45^0 cells are used for coplanar wire crossings.

QCA cells can be placed diagonally one after another to achieve inversion functionality. This is another fundamental logic structure used to obtain complex logic output.

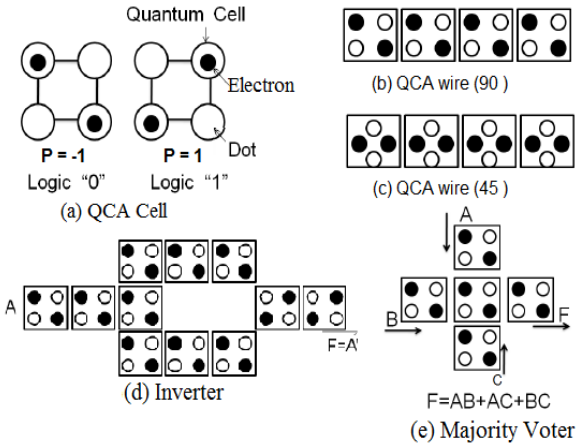

Fig. 1 The basic QCA Cells

Logical function of Majority Voter (MV) is described as MV (A, B, C) = AB + BC + CA. MV constituted by 5 QCA cells, as shown in Fig. 1(e). Logic AND and OR functions can be implemented from the MV by setting an input permanently to a 0 or 1 value.

A. QCA Clocking

Clock signals in QCA are produced by applying an electric field to the cells in order to either increase or decrease the tunnelling barrier between the dots in a QCA cell. Four clocking zones are available for use when pumping data down a circuit, as shown in Fig. 3. Each successive clocking signal is out of phase by 90 degrees with the previous one. Clocking scheme is adopted with four different phases known as switch, hold, release, and relaxes, as shown in Fig. 2.

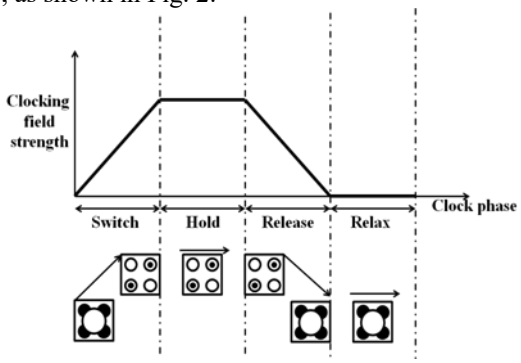

Fig. 2 QCA four clock phase

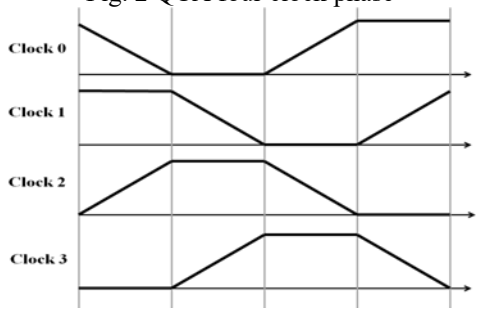

Fig. 3 QCA Clocking Zones

B. NAND-NOR-INVERTER (NNI)

Investigations of NNI gate have been conducted by Pijush Kanti Bhattacharjee (2010) [2]. It may be used to implement logical functions and has a lower overhead for initialising variables when implementing the fundamental logic gates. When compared to other gates like the Majority Voter (MV), And-Or-Inverter (AOI), and inverter (NOT), the NNI gate requires very little area. Fig. 4 depicts the Nand-Nor-Inverter gate, which is the consequence of implementing MV with the NOT function.

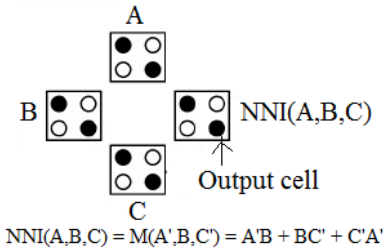

Fig. 4 QCA NNI Gate

The NNI gate is a universal gate and can be engaged for realizing flexible logic functions.

III. QCA Designer

The QCA layout editor and simulator are called QCA Designer. Circuit implementation is done using *QCADesigner Version 2.0.3*. This tool [3], estimates the power dissipation of QCA circuits. It uses the Coherence Vector Simulation Engine (CVSE) and Bistable Simulation Engine. The Coherence Vector Simulation Engine is one of the two built-in simulation engines in QCA Designer; it is slower than the Bistable Simulation Engine but produces more reliable results.

IV. RELATED WORK

The logic circuit can be designed using AND, OR, and NOR gates. There are also other gates presented to simplify the circuit such as XOR. Previously, designing the XOR circuit using QCA technology faced the wire crossing issue, as the main problem [4,5]. S. Santra and U. Roy [8], proposed the XOR gate implementation with Boolean expression and by using basic gates which reduces cell count compared to previous designs. Researchers have designed and proposed many XOR gate implementations [6,7]. However, all the prior implementations suffer from consuming a large area and delay (clock phases). These issues are attempted to be addressed in the current work. In 2015, Ajitha et al. [6] presented a new architecture of the QCA-XOR gate. Behrouz Safaiezadeh et al. (2021) designed an efficient novel structure of XOR gate. A novel 1-bit comparator circuit, 1-bit full adder, binary to gray and gray to binary converter are also designed and simulated based on the proposed XOR [9]. This gate has many limitations where one of its inputs is not reachable in one layer and the design required three clock phases delay.

V. PROPOSED DESIGN

A. XOR Gate

To design any arithmetic circuit and complex circuit XOR and XNOR gates are useful, since these gate are complex to fabricate with hardware usually ground as two input gates. From the previous research related to QCA technology, the XOR gate has drawn attention due to its importance in digital systems.

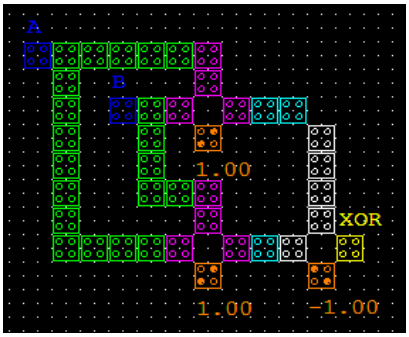

Fig. 5 QCA layout of the proposed XOR gate

Implementation of 2-input XOR gate in QCA has been depicted in Fig. 5, which was implemented by the minimum cell number and complexity and reached the output in one clock cycle with NNI gate configuration. The proposed 2-input XOR gate consists of 42 cells covering an area of 0.06 μm^2 (254nm×227nm). The simulation results of the 2-input XOR gate is presented in Fig. 6.

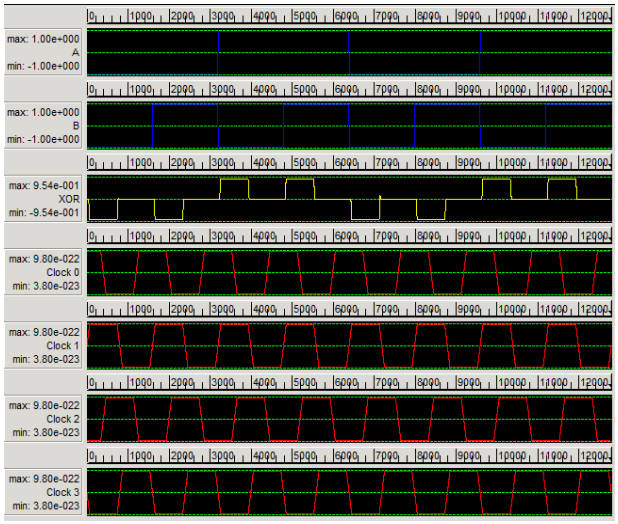

Fig. 6 Simulation results of the proposed design

B. Adder Design

The major arithmetical operations can be implemented by using adder circuit; adder circuit is classified as Half Adder (HA) and Full Adder (FA). In this section we implemented HA and FA by using the proposed XOR gate.

Based on Fig. 7, the half adder is made up of 4 majority gates and 2 inverters. A half adder can be implemented using only 77 cells and an area of 83160 nm2, which is significantly smaller than previous implementations. Fig. 8 shows the simulation result of half adder circuit.

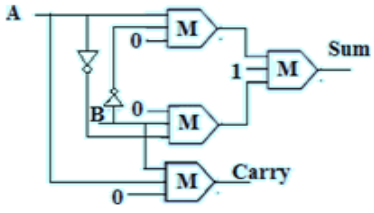

Fig. 7 Half Adder Schematic

Fig. 8 Simulation Result of Half Adder

Full adders are directly designed using the QCA addition algorithm. Fig. 9 depicts the direct reduction technique used to design the full adder using three majority gates and two inverters. Fig. 10 depicts the corresponding QCA simulation result. Cells needed for the QCA implementation is 98, with a total area of 100,800 nm^2, which is less than former implementations.

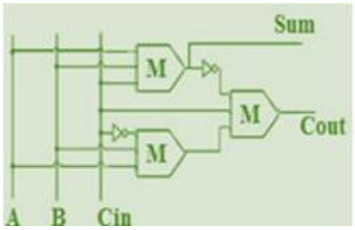

Fig. 9 Full Adder Schematic

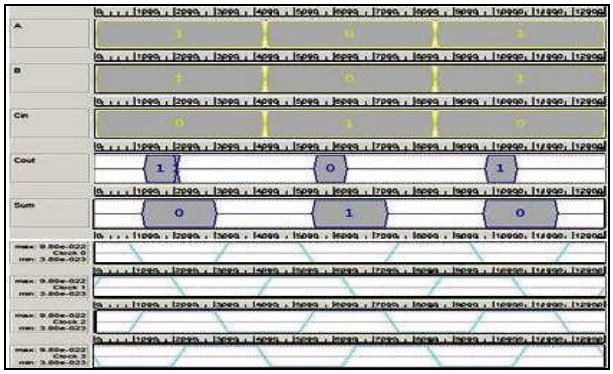

Fig. 10 Simulation Result of Full Adder

C. Subtractor Design

As can be seen in Figure 5.15, the half subtractor consists of four majority gates and three inverters. In Fig. 11, we can see "the corresponding QCA" implementation. In our implementation, we need a total of 77 cells, covering an area of 83160 nm^2.

Fig. 12 depict QCA cells performing the subtractor's function. There must be 98 cells totaling 100,800 nm^2 in size for the QCA to function properly.

The waveforms of a simulated half subtractor and full subtractor can be seen in Fig. 13 and Fig. 14, respectively. The subtractors, just like the adder, needed four clock zones in order to create the necessary output.

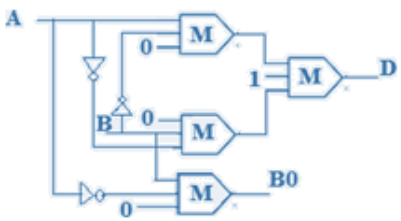

Fig. 11 Half Subtractor Schematic

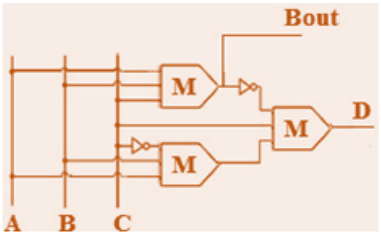

Fig. 12 Full Subtractor Schematic

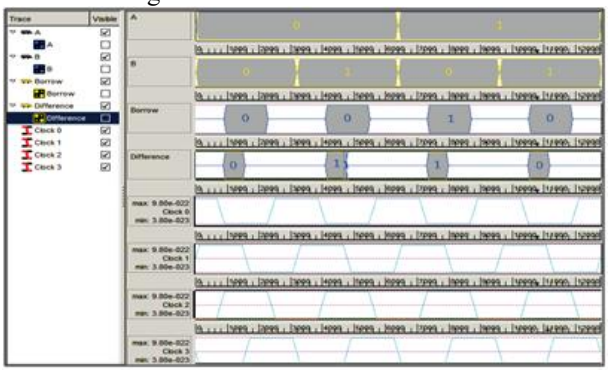

Fig. 13 Simulation Result of Half Subtractor

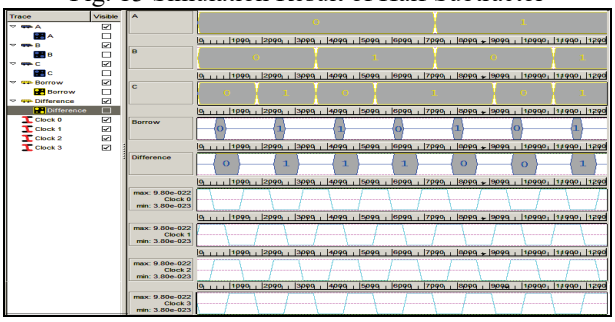

Fig. 14 Simulation Result of Full Subtractor

VI. CONCLUSION

An efficient XOR gate in QCA can vastly improve efficiency in computational circuits. The XOR gate is optimized and the cell count is reduced.

This paper represents the design, layout and simulation of combinational circuits based on prpoosed XOR circuit configuration. An optimal design for XOR base half adder, full adder, half subtractor and full subtractor circuits has been proposed. The proposed circuits are simulated using QCA based circuits simulation tools i.e. QCA Designer [3]. This design is efficient in terms of cell count, area. Moreover considering the less numbers of cell count can presume that power consumption in such a circuit will obviously be low. The novelties of the XOR gate besides parameter like delay, majority gate, and area are minimal in comparison to other design as proposed [8].

Tables I comparison between the proposed XOR gate, Half adder, Full-adder, Half subtractor and Full subtractor in QCA technology with the previous works.

Table I Comparison of XOR gate,

Logical Structures	Previous Logical Structures using MG		
	Complexity	Area	
XOR	87cells	315nmx290nm	
Half adder	105cells	300nmx360nm	
Full adder	137cells	435nmx300nm	
Half subtractor	112 cells	377nmx297nm	
Full subtractor	114cells	381nmx300nm	

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cellular automata: the physics of computing with arrays of quantum dot molecules", Proceedings Workshop on Physics and Computation. PhysComp '94, pp. 5-13, doi: 10.1109/PHYCMP.1994.363705, 1994.

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